Design and Implementation of Demodulator and Carrier Phase Compensation System for Satellite Communication

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Abstract

A proposed design and FPGA implementation of a demodulator and phase compensation system is presented.The system is simple, accurate, dissipate low power. Simulations indicate that the proposed system compensates the error in the received phase quickly which decreases the bit error rate (BER) in wireless systems. FPGA implementation of the proposed system shows a power reduction by 27.91% and the speed by 66.89% compared to Costas loop.

Keywords: Phase shift keying; Phase Compensation; Phase locked loop; Costas loop; Field programmable gate array.

1. Introduction

Digital modulation is the process of translating a digital information into the amplitude, phase, or frequency of the transmitted signal. The modulation algorithm bounded many bits into one symbol, and the symbol transmission rate determines the bandwidth of the transmitted signal. Having a large number of bits per symbol generally yields a higher data rate for a given signal bandwidth. However, the larger the number of bits per symbol, the greater the required received signal to noise ratio (SNR) for a given target Bit Error Rate (BER).

Phase shift keying (PSK) is a modulation technique in digital communication systems such as satellite communications. In this type of modulation, data located the phase of received signal. The challenge in the design process of the receiver in this type of modulation is identifying small changes in incoming phase in short time [1]. When a different in phase occurred between the two voltage-controlled oscillators (VCO) in both transmitter and receiver, a compensation of phase shift must be performed for the received signal before demodulation. Different phase compensation methods are done such as feedforward and feedback methods.

Feedforward algorithm perform phase correction depending on mathematical operations which requires a complex hardware implementation and suffers from high power consumption and slow operation [2]. Feedback algorithm depend on previous output to compensate the phase changes,

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such as Costas loop which work in a similar way as phase locked loop (PLL) is shown in figure 1 [3-10].

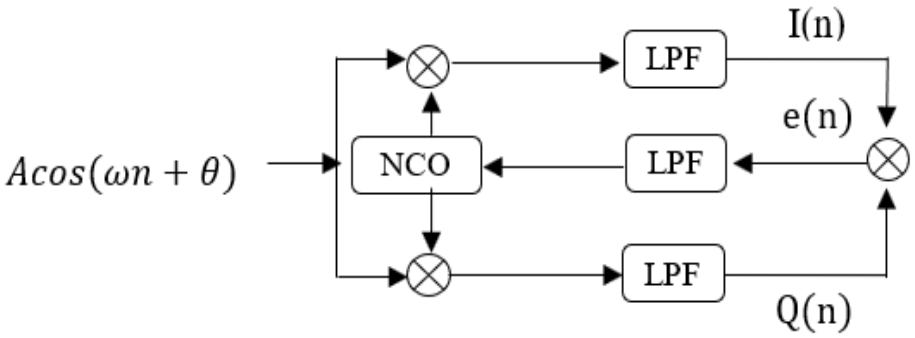

Figure 1: Digital Costas loop

As noticed in figure 1.the received signal multiplied by the generated NCO signal into two arms; upper arm and lower arm. Both arms generate a signal I(n) and Q(n) respectively after passing through low pass filter (LPF) low pass filter (LPF). After multiplying both signals I(n) and Q(n) a control signal is generated to control the generated phase of NCO signal. The Costas loop suffers from internal frequency ripples [11], long settling time [12-13], and high-power consumption.

Different attempts to solve high power consumption are presented in [14-16]. The idea of reducing frequency acquisition and lock detection presented in [17]. Unfortunately, all the previous attempts take care of one drawback and neglect the others so it is important to propose a new algorithm or solve all the drawbacks of conventional Costas loop.

2. Proposed Algorithm

This research introduces a novel mathematical model and implementation for multi-phase shift keying demodulation and phase compensation, the block diagram of the proposed system is shown in figure 2. It is noticed that the proposed system does not contain a loop filter or multipliers which considers a method to ensures simplicity and stability of the system. The detector block, computes the sign of the estimated phase. It receives the quadrature input signal and the quadrature generated signal from NCO component. In phase calculation component mathematical equations are performed and the result is passed to NCO to control increasing/ decreasing of the generated phase.

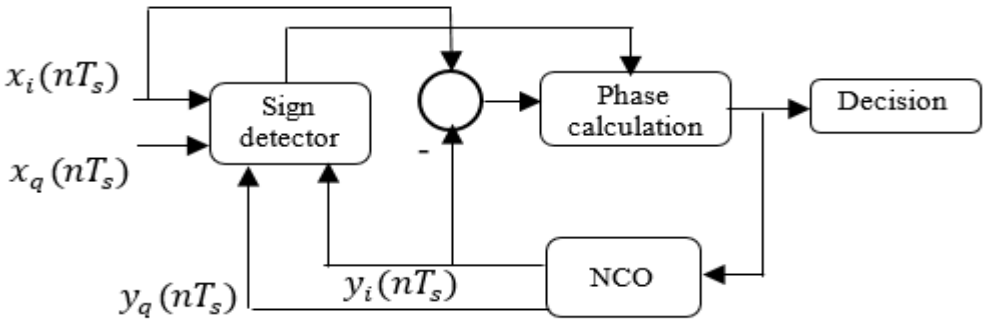

Figure 2: Proposed PSK phase compensation system

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NCO component produces a sine and cosine signals with zero phase and specific frequency according to CORDIC algorithm [18]. Figure 3 shows a CORDIC algorithm flow chart.

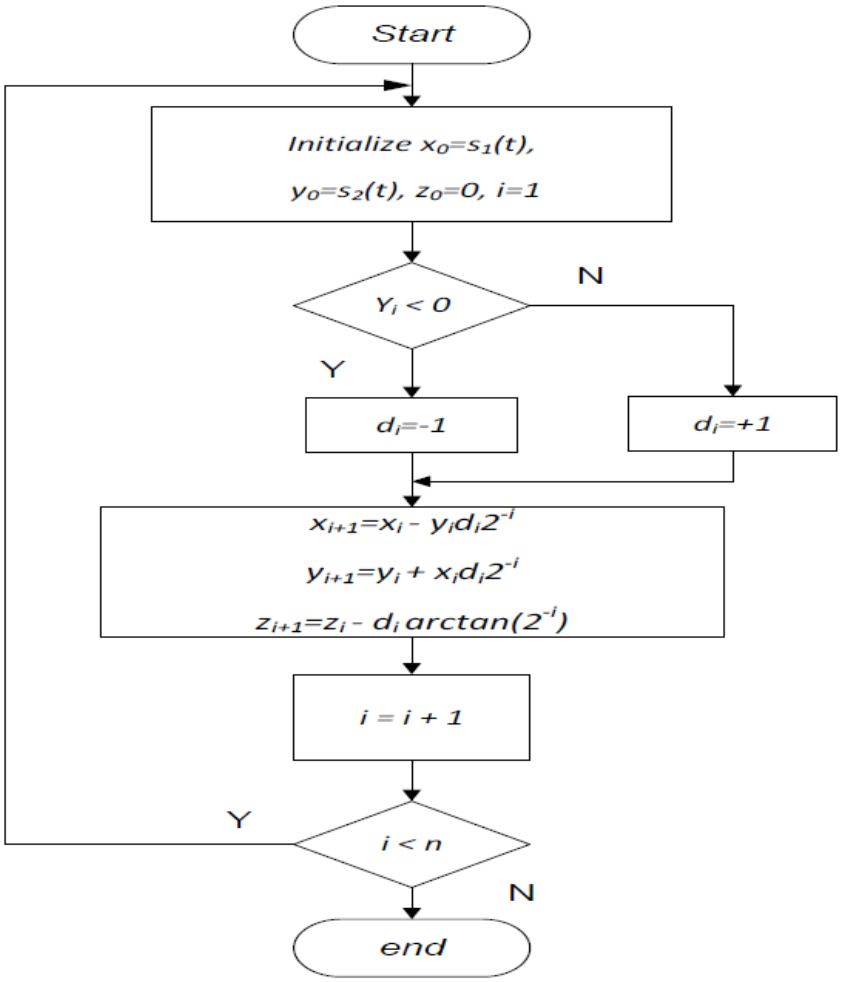

Figure 3: CORDIC algorithm flowchart

The result of subtraction $(x_i(n) - y_i(n))$ is a sinusoidal with amplitude proportional to the phase difference between the NCO phase and the phase of the received input signal. A detector is used to find the amplitude of the sinusoidal signal. The input MPSK modulated quadrature signal is :

$$x_i(nT_s) = A\cos(\omega nT_s + \theta + \phi) \quad (1)$$

$$x_q(nT_S) = A\sin(\omega nT_S + \theta + \phi) \quad (2)$$

Where

$$A = \sqrt{\frac{2E_S}{T_{ss}}},\ \theta = \frac{2\pi}{M}$$

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ϕ: input phase shift (rad).

T_{ss}: symbol time (s).

T_s: sampling time (s).

ω: radian frequency of the carrier (rad/s).

M: number of symbols.

E_S: signal energy (J).

The generated quadrature NCO signal is

$$y_i(nT_s) = B\ cos(\omega nT_s + \hat{\theta}) \quad (3)$$

$$y_q(nT_s) = B\ sin(\omega nT_s + \hat{\theta}) \quad (4)$$

Where

B is the amplitude

$\hat{\theta}$ generated NCO phase

$$sign(\hat{\theta}) = sign[x_q(nT_S) \times y_i(nT_s) - x_i(nT_s) \times y_q(nT_S)] \quad (5)$$

$$e(nT_s) = x_i(nT_s) - y_i(nT_s)$$

$$e(nT_s) = A\cos(\omega nT_s + \theta) - B\cos(\omega nT_s + \hat{\theta}) = C\cos(\omega nT_s + \phi) \quad (6)$$

$$[A\cos(\theta) - B\cos(\hat{\theta}) - C\cos(\phi)]\cos(\omega nT_s) = [A\sin(\theta) - B\sin(\hat{\theta}) - C\sin(\phi)]\sin(\omega nT_s) \quad (7)$$

$$C^2\ cos^2(\phi) = A^2\ cos^2(\theta) + B^2\ cos^2(\hat{\theta}) - 2AB\ cos(\theta)cos(\hat{\theta}) \quad (8)$$

$$C^2\ sin^2(\phi) = A^2\ sin^2(\theta) + B^2\ sin^2(\hat{\theta}) - 2AB\ sin(\theta)sin(\hat{\theta}) \quad (9)$$

Adding (8) and (9) will be

$$c^2[cos^2(\phi) + sin^2(\phi)] = A^2[cos^2(\theta) + sin^2(\theta)] + B^2[cos^2(\hat{\theta}) + sin^2(\hat{\theta})] - 2AB[cos(\theta)\ cos(\hat{\theta}) + sin(\theta)sin(\hat{\theta})]$$

$$C^2 = A^2 + B^2 - 2ABcos(\theta - \hat{\theta})$$

$$C = \sqrt{A^2 + B^2 - 2AB\ cos(\theta - \hat{\theta})} \quad (10)$$

If A=B

$$C = A\sqrt{2}\sqrt{1 - \cos(\theta - \hat{\theta})} \quad (11)$$

$$\cos(\theta - \hat{\theta}) = (1 - \frac{C^2}{2})$$

$$(\theta - \hat{\theta}) = \cos^{-1}(1 - \frac{C^2}{2})$$

In case of small phase drift

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$$(\theta - \hat{\theta}) = C^2 \quad (12)$$

Initially $\hat{\theta} = 0$

So, $c^2 = \theta$ (13)

3. Matlab Simulations

A received binary phase shift keying signal with a phase shift of 45^o and signal to noise ratio 10 dB is applied to both conventional method, and proposed system. Figure 4 shows the constellation diagram and bit error rate (BER) range for both systems.

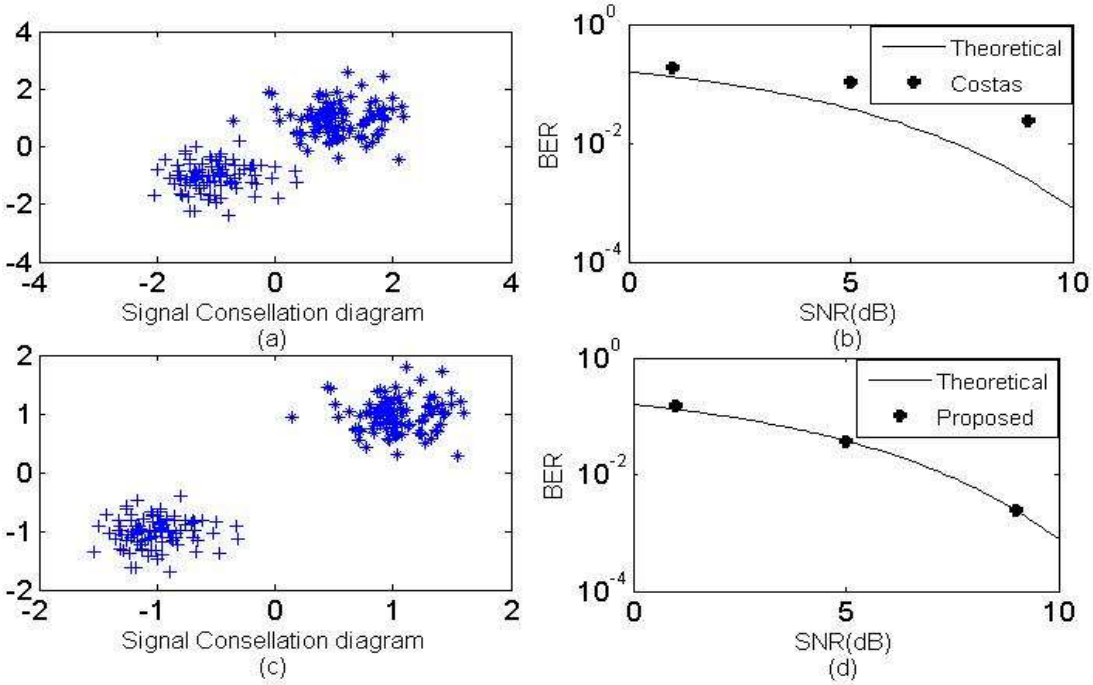

Figure 4: (a)constellation when using costas loop (b) BER when using costas loop (c)constellation when using proposed system (b) BER when using proposed system.

In case of a quadrature phase shift keying signal with a phase shift of 22.5^o and figure 5 shows the constellation diagram and bit error rate (BER) range for both systems.

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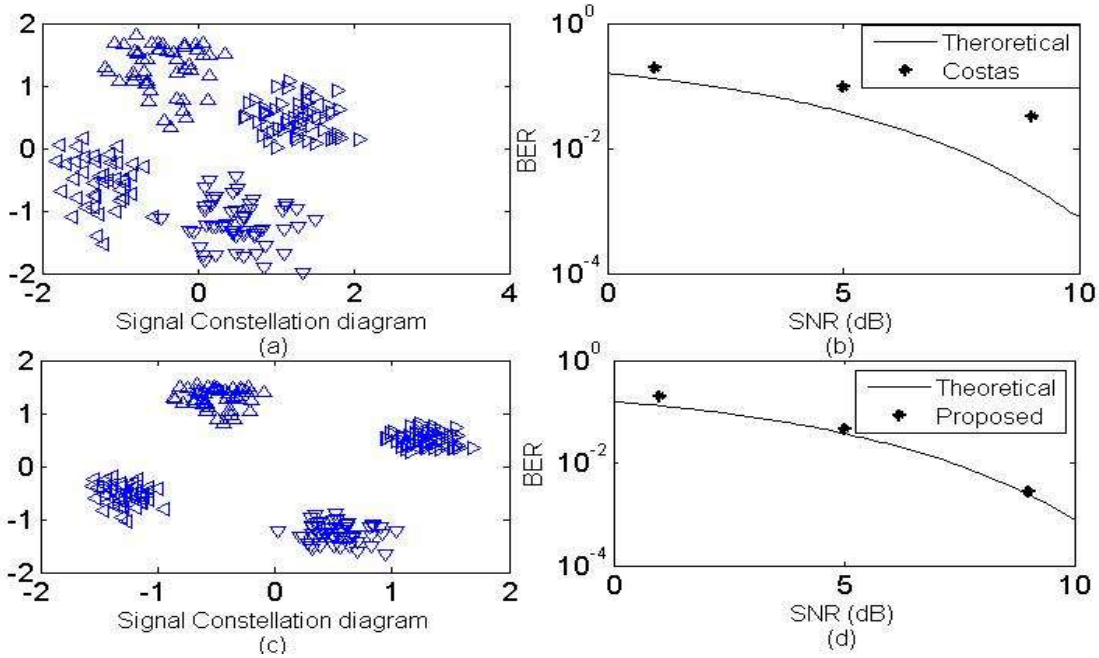

Figure 5: (a)constellation when using costas loop (b) BER when using costas loop (c)constellation when using proposed system (b) BER when using proposed system

In case of a 8- phase shift keying signal with a phase shift of 22.5^{o} and figure 6 shows the constellation diagram and bit error rate (BER) range for both systems. While, figure 7 shows a constellation diagram in case of 16-phase shift keying, phase shift 22.5^{o} rad, and SNR=15dB.

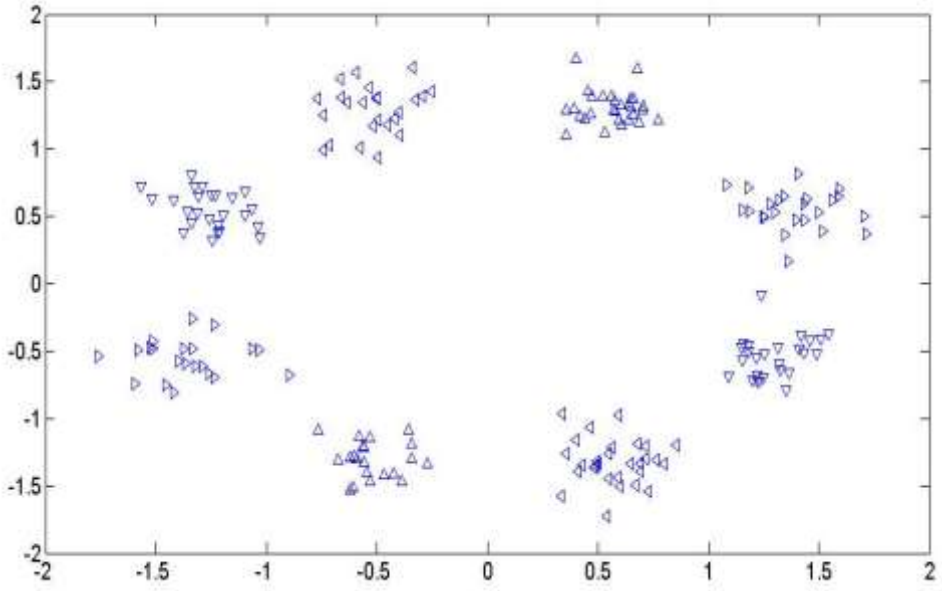

Figure 6: Constellation diagram for 8-PSK modulation

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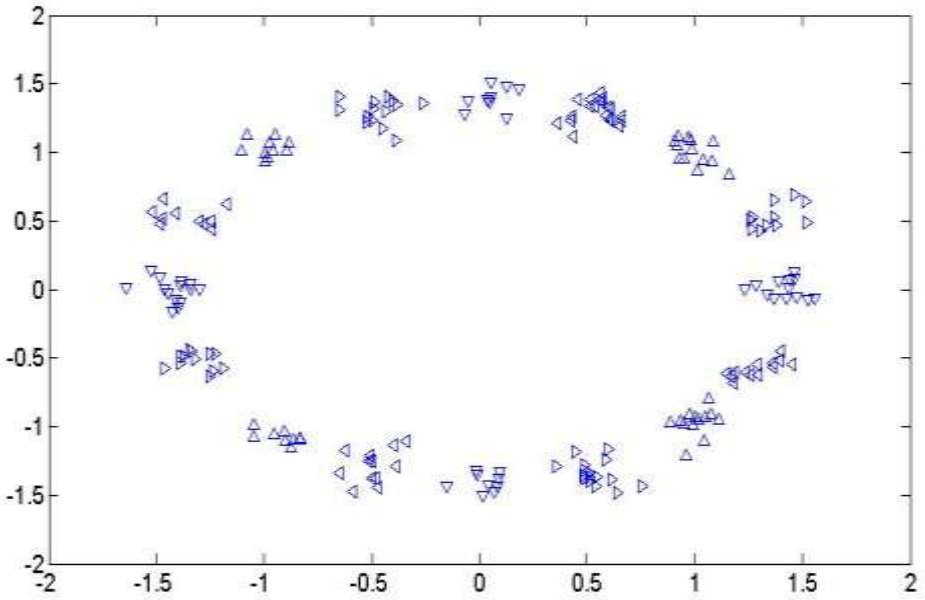

Figure 7: Constellation diagram for 16-PSK modulation

4. Hardware Results

The proposed system is modeled using the Xilinx system generator tool [19]. All signals of are fixed point signals with 16 bits. Figure 8 shows the system model in a Xilinx system generator environment. The model receives input modulated quadrature signals $x_i(n)$, $xq(n)$ with AWGN. Each block of the proposed system is shown in figure 9, and figure 10.

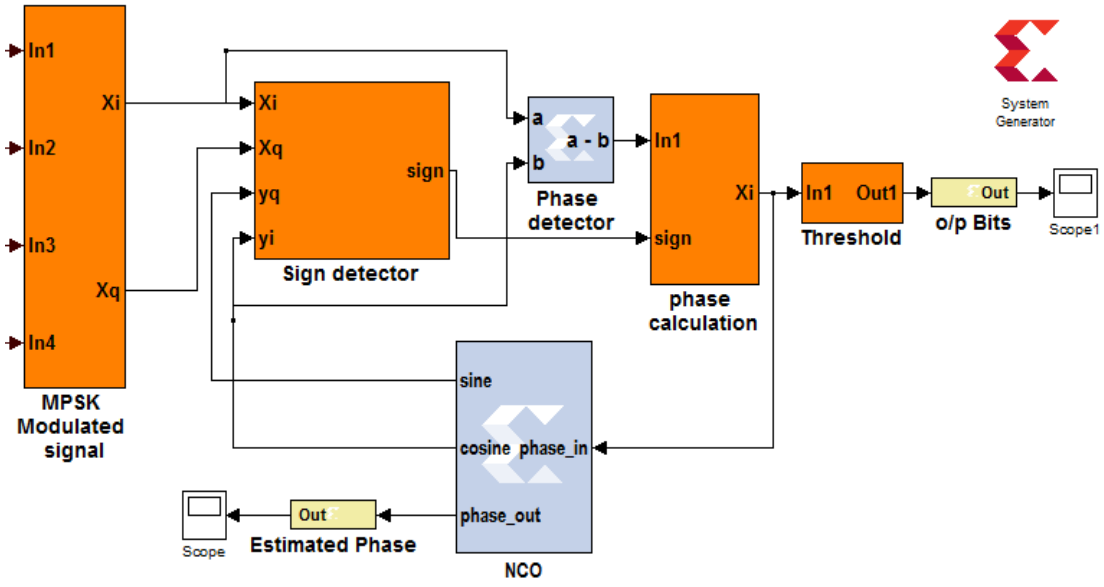

Figure 8: Hardware model of proposed system

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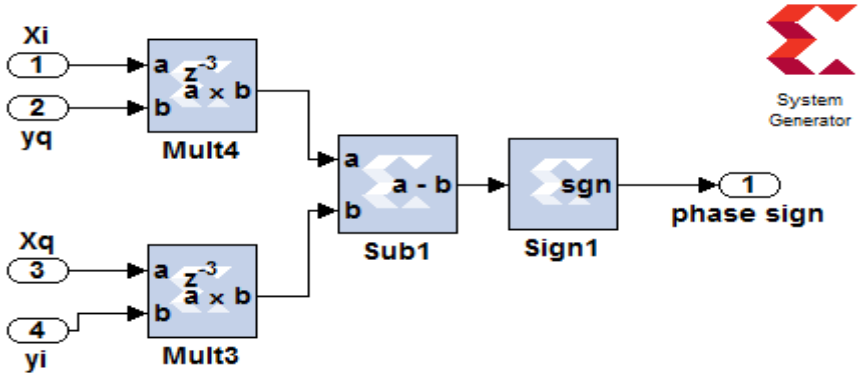

Figure 9: "sign detector" block.

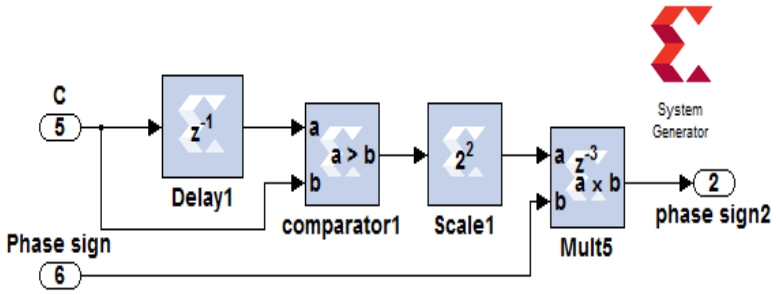

Figure 10: "phase calculation" block

The proposed system, and traditional Costas loop system are implemented using DSP board [20-28]. A scatter plot for QPSK demodulated signal at signal to noise ratio 10 dB is shown in figure 10. The FPGA consumed resources are shown in table 1.

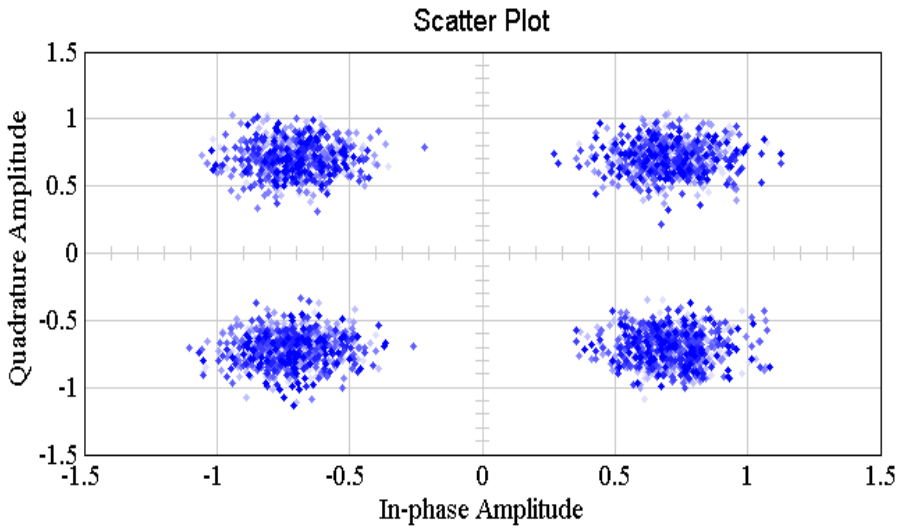

Figure 11: Scatter plot for QPSK at SNR= 10 dB

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Table 1: FPGA Consumed Resources

Component	Proposed	Costas	Available
slice flip flops	**125**	**292**	**33280**
4 input LUTs	**350**	**471**	**33280**
bonded IOBs	**50**	**50**	**519**
Operating frequency	**175 MHz**	**118 MHz**	
Power	**275 mW**	**985 mW**	

5. Conclusion

A novel and accurate MPSK demodulator, and phase compensation is designed and implemented in this paper. Simulations examines the performance of the proposed method with Costas loop. The proposed system reduced the phase estimation time, BER, power consumption with simple structure which make it suitable for satellite communication.

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Conflicts of Interest: "The authors declare no conflict of interest."

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