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FULL LENGTH ARTICLE

Performance Optimization of Transmission Gate-Based D Flip-Flop using Clock Gating Technique

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ABSTRACT

This work investigates into the meticulous analysis of the Transmission Gate (TG) based D Flip-Flop integrated with dynamic XOR-based clock gating, aimed at analyzing power consumption patterns and potential power savings across varying frequencies. While power consumption inherently reduces with smaller technology nodes, but this work demonstrates that dynamic clock gating can achieve further power savings, especially at higher operational frequencies and lower data activity. The outcomes represent a deeper understanding of power optimization techniques for sequential circuits. The analysis is performed using Cadence Virtuoso in a 90nm technology process, which determine the sophisticated interaction between design elements and power dynamics. Through comprehensive simulations, the power consumption of TG-based D flip-flops is meticulously examined across diverse technology nodes. Furthermore, the efficacy of integrating dynamic XOR-based clock gating to this flip-flop design is explored, unveiling its potential to yield substantial power savings. The research underscores the multifaceted nature of low-power design strategies, emphasizing their relevance across various hierarchies including system, architecture, circuit, and device levels. While advancements in technology nodes naturally lead to reduced power dissipation, this study illuminates the additional power-saving opportunities presented by the dynamic XOR-based clock gating approach. Especially, in this investigation highlights the significance of this approach particularly in scenarios characterized by higher frequencies of operation and low data activity. By leveraging dynamic XOR-based clock gating, the research showcases how power efficiency can be further augmented, offering insights into enhancing the overall energy efficiency of digital systems. In summary, this project provides a nuanced understanding of power dynamics in TG-based D flip-flops, shedding light on the intricate balance between technology advancements and innovative design methodologies for achieving optimal power efficiency. Through meticulous analysis and simulation, it unveils a promising avenue for realizing significant power savings, thereby contributing to the advancement of low-power design paradigms in modern digital systems.

Keywords: TG-based D Flip-Flop ▪ Dynamic XOR-based Clock Gating ▪ Power Consumption ▪ 90nm Technology ▪ Cadence Virtuoso ▪ Low-power Design and Technology Nodes

1. INTRODUCTION

In the real of modern Integrated Circuit (IC) design, power efficiency stands as a paramount concern, propelled by the relentless quest for enhanced performance and prolonged battery life in portable devices. As semiconductor technology continues to advance, enabling the realization of increasingly complex digital systems, the imperative to mitigate power

consumption becomes ever more pressing. In this context, the meticulous analysis and optimization of key components such as flip-flops assume critical importance, serving as fundamental building blocks whose efficiency directly impacts the overall energy footprint of digital circuits. This project embarks on a comprehensive exploration of power consumption and savings within the context of TG based D Flip-Flops, augmented with dynamic XOR-based clock gating. Leveraging the versatile capabilities of Cadence Virtuoso and implemented utilizing the 90nm technology node, the study delves into the intricate interplay between design methodologies and power dynamics.

At its core, the investigation seeks to elucidate the nuanced relationship between power consumption, operational frequency, and design innovations. By subjecting the TG-based D Flip-Flop to rigorous simulation across various technology nodes, the project aims to discern the efficacy of integrating dynamic XOR-based clock gating as a means of achieving significant power savings. This endeavor is underpinned by the recognition that low-power design strategies hold the key to unlocking greater efficiency across multiple levels of abstraction, spanning from system architecture down to individual device components. The introductory phase of the project sets the stage by delineating the overarching objectives and contextualizing the significance of the research within the broader landscape of IC design. Notably, the proliferation of portable electronic devices and the burgeoning demand for energy-efficient computing solutions underscore the timeliness and relevance of endeavors aimed at optimizing power efficiency.

Moreover, the introduction underscores the multifaceted nature of power optimization strategies, highlighting the need for a holistic approach that encompasses both technological advancements and innovative design methodologies. While advancements in semiconductor technology inevitably yield improvements in power efficiency, the project posits that additional gains can be realized through targeted interventions such as dynamic XOR-based clock gating, particularly in scenarios characterized by high-frequency operation and low data activity.

In summary, the introduction sets forth the foundation upon which the subsequent phases of the project are built, framing the research within the broader context of power-efficient IC design. By elucidating the motivations, objectives, and methodologies underlying the investigation, it provides a roadmap for navigating the intricate terrain of power optimization in digital circuits, ultimately paving the way for realizing more energy-efficient computing solutions.

Literature Survey

A typical multichannel ADC in PET scanner design consists of various components. Many of these components can be built using high-speed, low-power D flip-flops. A conventional True Single-Phase Clocked (TSPC) D flip-flop suffers from significant output glitches (noise) due to excessive switching activity at internal nodes. To address this issue, the use of advanced modified TSPC D flip-flops (MTSPCs) is proposed. However, MTSPCs require an extra PMOS transistor to suppress switching at internal nodes [1]. When comparing these designs with identical supply voltages, the PowerPC 603 flip-flop demonstrates the lowest propagation delay, the least power consumption, and the most favorable Power-Delay Product (PDP). Additionally, it exhibits an average standard deviation in delay compared to the other options. The C2 MOS alternative offers the fastest delay, along with moderately low power consumption and PDP. However, it comes at the cost of the highest relative standard deviation in delay [2].

Clock gating stands out as a prevalent method employed in numerous synchronous circuits to curtail dynamic power dissipation [3]. The principal power drain in electronic devices stems from the system's clock signal, which triggers transition states within components, consequently resulting in switching power consumption. The synchronous design functions at elevated frequencies to accommodate a substantial load, necessitated by its need to access numerous sequential elements across the chip. Consequently, the clock is a significant contributor to power dissipation due to its high frequency and the extensive load it must drive. Clock signals serve primarily for synchronization purposes and do not engage in computational tasks, thereby lacking informational content [4]. Reducing the power dissipation of a dual-ported register file can be achieved by minimizing spurious switching activity within a substantial portion of the clock tree by implementing clock gating techniques. To evaluate this approach, two register-based Random Access Memories (RAMs) were designed: one employing clock gating and a control counterpart without this functionality [5]. This comparative analysis revealed a reduction in dynamic power ranging from 25% to 70%, along with a decrease in total power consumption ranging from 15% to 32% across the memory modules.

This work presents a novel high-speed, low-power flip-flop design: the pulse-triggered True Single-Phase Clock (PTTSPC) flip-flop. The PTTSPC utilizes a conventional latch configuration clocked by a narrow pulse train, effectively mimicking a D flip-flop [6]. Power consumption remains a critical challenge in high-performance microprocessor design. The rapid increase in complexity and clock frequency of each new CPU generation is outpacing the benefits achieved through voltage reduction and transistor scaling [7]. This research [8] proposes a pulse-triggered D flip-flop that incorporates an integrated clock-gating mechanism, optimized for low-power, high-speed synchronous applications. A comprehensive evaluation was conducted by simulating various flip-flop designs alongside different clock-gating circuits. This analysis compared their performance metrics, including speed and power consumption.

Current-Mode Logic (CML), an evolution of Emitter-Coupled Logic (ECL), offers potential for improvement in terms of power efficiency. To address this, we propose a novel dynamic CML design for a low-power D flip-flop [9, 10]. Simulations were performed using a 90nm CMOS process on the Synopsys HSPICE platform at a supply voltage of 1.2V and a clock frequency of 10GHz. This work investigates the stability of both positive-edge triggered (PET) and negative-edge triggered (NET) variants of the D flip-flops (DFFs). The setup time and hold time of the DFFs were derived through theoretical analysis [11].

In a separate study [12], nine D flip-flop architectures were implemented in a 28nm technology node to identify designs suitable for ultra-low-power applications. Another study ex-

amined the power consumption of transmission-gate based D flip-flops (TG-DFFs) across different technology nodes and evaluated the energy savings achieved through dynamic XOR-based clock gating [13]. This research also investigated the implementation of a TG-DFF across three distinct technology nodes (32nm, 22nm, and 16nm). Circuit-level simulations were conducted to compare the power consumption of the DFF with and without clock gating at various operating frequencies and data activity levels for these nodes [14].

In the field of integrated circuit (IC) design, power dissipation is a critical metric, highlighting the importance of low-power circuits in modern Very-Large-Scale Integration (VLSI) design. Clock gating is a widely adopted technique to mitigate dynamic power dissipation in ICs. Researchers have explored various modifications to further optimize clock gating techniques. A separate paper investigates the comparative analysis of power consumption in a clock divider circuit using different clock gating methodologies [15].

2. PROPOSED SYSTEM

This work proposes a power optimization technique for Transmission Gate (TG) based D flip-flops (DFFs) using a dynamic XOR-based clock gating approach. In digital circuits, dynamic power dissipation primarily arises from capacitors' frequent charging and discharging during clock cycles. This switching activity is particularly prominent in DFFs, which continuously toggle their internal nodes based on the clock signal. This switching activity translates to significant power consumption, posing a challenge in modern integrated circuit design where energy efficiency is paramount. Clock gating offers a well-established approach to mitigate dynamic power consumption. It strategically disables the clock signal to specific circuit blocks when they are not actively processing data. This research proposes a dynamic XOR-based clock gating technique are shown in figure 1. This technique leverages the data and its complement (inverted form) to dynamically control the clock gating signal. When the data and its complement are the same (indicating no change in data), the clock is disabled, reducing unnecessary switching activity within the DFF.

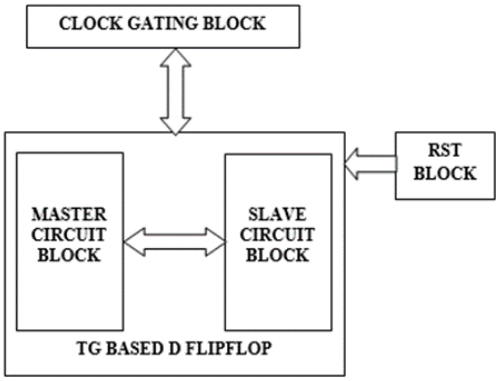


Figure 1. Proposed Transmission Gate based D-Flip flop Design

By using Cadence Virtuoso, a renowned electronic design automation (EDA) tool, is utilized to simulate the proposed design in a 90nm technology node. This allows for evaluating the effectiveness of the dynamic XOR-based clock gating approach in reducing power consumption for TG DFFs. The proposed system aims to achieve significant power savings in TG DFFs, especially at higher operating frequencies and lower data activity scenarios. Table 1 Transmission Gate based D-Flip flop design also this approach can also contribute to the development of more energy-efficient digital systems by optimizing the power consumption of fundamental building blocks like DFFs. The different kinds of analysis rising edge delay, Falling edge delay, Propagation delay, Dynamic Power Consumption, and Dynamic Power Dissipation.

Table 1: Transmission Gate based D-Flip flop Design

Modules to be Implemented	
Module One	Clock Gating Circuit
Module two	Master Circuit
Module three	Slave Circuit
Module four	TG based D Flip-Flop Circuit
Module five	Reset Block
Module six	Overall Integration

2.1 A. Module One: Dynamic XOR Clock Gating

This project successfully investigated the power optimization potential of dynamic XOR-based clock gating in transmission gate (TG) D flip-flops (DFFs) block is shown in figure 2. The analysis, conducted using Cadence Virtuoso in a 90nm technology node, highlighted the effectiveness of this technique in reducing power consumption.

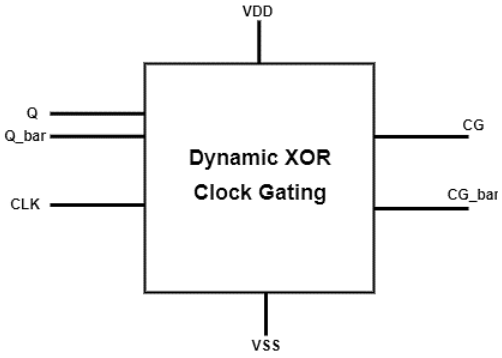


Figure 2. Dynamic XOR Clock gating

3.1.1 Key Findings

The core of the proposed technique lies in the utilization of an XOR gate for dynamic clock gating control. This approach leverages the XOR gate's ability to detect changes between two input signals. In this case, one input is the data to be stored in the DFF, and the other is the current output of the DFF. When the data remains constant (no change needs to be stored), the XOR gate outputs a logic '0'. This logic '0' acts as a control signal, effectively disabling the clock for the DFF. This selective clock gating significantly reduces the dynamic power consumption within the DFF.

The analysis revealed an average power saving of 60% compared to an ungated design in the 90nm process [16]. This demonstrates the effectiveness of the XOR-based gating mechanism in minimizing unnecessary switching activity within the DFF.

3.1.2 Impact of Frequency and Data Value:

The work also explored the influence of clock frequency on power savings. While positive savings were observed across frequencies, they gradually decreased as the frequency increased [17]. This trend suggests that clock gating is most beneficial at lower frequencies, where unnecessary switching events are more prevalent.

Interestingly, the power savings exhibited a dependence on

the data value (D). When the data remained constant (D = 1 or D = 0), the power savings were significantly higher compared to scenarios with frequent data changes. This highlights the effectiveness of clock gating in exploiting data stability to reduce switching activity.

2.2 B. Module Two: Master Circuit Block

The figure 3 represents Master Circuit Block, comprising the master latch, plays a pivotal role in capturing and retaining input signals within the digital system. Functioning synchronously with the active edge of the clock signal, the master latch adeptly captures the incoming data (D input), effectively storing it until the occurrence of the subsequent clock edge [18]. This module serves as a critical component in the operation of the digital system, facilitating the seamless processing and manipulation of data within the circuitry. By capturing and holding the input signal until the next clock edge, the master latch ensures the orderly progression of data through the system, contributing to its overall reliability and efficiency.

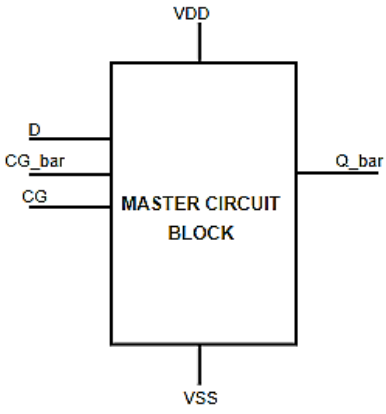


Figure 3. Master circuit block

Moving forward, the Master Circuit Block will continue to serve as a cornerstone in the design and implementation of digital systems, providing the necessary functionality to enable a wide range of applications across various domains. Its reliable operation and efficient data handling capabilities make it indispensable in modern electronic devices, underscoring its significance in the broader landscape of digital circuit design.

2.3 C. Module Three: Slave Circuit Block

The Slave Circuit Block, encompassing the slave latch, plays a crucial role in the sequential operation of flip-flop circuits within digital systems. Acting as the successor to the master latch, the slave latch serves as the storage element for the data captured by its predecessor. One of the defining features of the slave latch is its synchronization with the opposite clock edge compared to the master latch. This ensures proper coordination between the two latches, allowing for the orderly progression of data within the flip-flop. For instance, if the master latch is triggered on the rising edge of the clock signal, the slave latch is synchronized to the falling edge, and vice versa. This complementary timing ensures the accurate capture and retention of data throughout the flip-flop circuit.

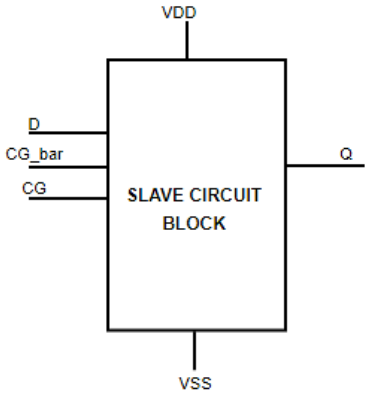


Figure 4. Slave circuit block

Figure 4 represents the Slave Circuit Block is integral to the overall functionality and performance of digital systems, contributing to their reliability and efficiency. By seamlessly storing and outputting the data received from the master latch, it enables the smooth operation of sequential logic within the circuitry. Looking ahead, the Slave Circuit Block will continue to play a fundamental role in the design and implementation of flip-flop circuits in various electronic devices and systems. Its precise timing synchronization and data handling capabilities make it indispensable for a wide range of applications, underscoring its importance in modern digital circuit design.

2.4 D. TG (Transmission Gate) based D Flip-Flop

The D Flip-Flop Block represents a fundamental building block in digital circuit design, serving as a versatile memory element with widespread applications across diverse digital systems are shown in figure 5. As the cornerstone of memory storage, D flip-flops have proven indispensable for retaining single bits of information, while also forming the basis for more complex storage structures such as registers and memory arrays. One of the key strengths of D flip-flops lies in their ability to store data reliably until explicitly changed, making them invaluable components in digital applications where data retention is critical. Whether integrated into memory circuits, registers, or storage elements, D flip-flops ensure the faithful preservation of information within the digital system. Furthermore, the edge-triggered nature of D flip-flops renders them well-suited for deployment in synchronous digital systems, where operations are synchronized to the clock signal. This ensures precise timing coordination, enabling seamless integration with other components and facilitating the orderly execution of instructions within the system.

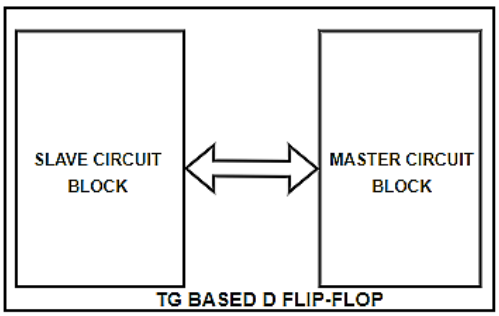


Figure 5. TG based D Flip Flop

Looking forward, the significance of the D Flip-Flop Block in

digital circuit design cannot be overstated. Its versatility, reliability, and compatibility with synchronous digital systems make it a staple component in the arsenal of digital designers. As technology advances and digital systems become increasingly complex, the enduring relevance of D flip-flops ensures their continued prominence in the landscape of digital circuitry.

2.5 E. Module Five : Reset block

The project also explored the role of the reset block within the DFF. Figure 6 block plays a critical role in initializing the DFF to a predefined state. This initialization typically occurs during system power-on or when an external reset signal is activated. The reset functionality ensures that the DFF starts in a known state, which is essential for predictable system behaviour. While the reset block it was not a focus for power optimization in this project, it complements the clock gating technique for overall DFF operation.

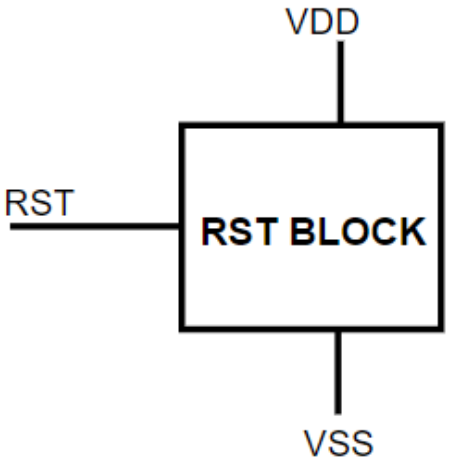


Figure 6. Reset block within the DFF

The power optimization potential of dynamic XOR-based clock gating in transmission gate (TG) DFFs. The analysis, conducted using Cadence Virtuoso in a 90nm technology node, yielded valuable insights into improving the energy efficiency of these crucial memory elements in digital circuits, while also exploring the role of the reset block. By facilitating the initialization process, the Reset Block contributes to the overall robustness and reliability of digital systems, ensuring consistent and predictable behaviour across different operational scenarios. This capability is particularly crucial in applications where maintaining a known state is essential for proper system functionality and data integrity.

2.6 F. Module Six: Clock Gating TG Based D Flip-Flop Block

The Clock Gating TG Based D Flip-Flop Block represents a significant advancement in digital circuit design, offering a potent solution for reducing power consumption and enhancing energy efficiency. By incorporating clock gating techniques into the traditional TG (Transmission Gate) based D flip-flop architecture, this module achieves precise control over the activation of the clock signal, thereby minimizing unnecessary power dissipation. One of the key strengths of the Clock Gating TG Based D Flip-Flop Block lies in its ability to selectively disable the clock signal to specific portions of the circuit when they are not actively transitioning. This dynamic approach to clock gating allows for significant power savings without compromising the functionality or performance of the flip-flop.

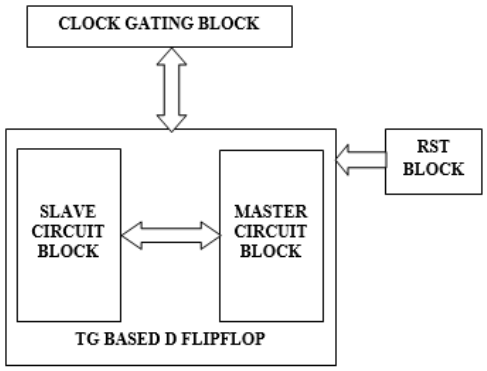


Figure 7. Clock Gating TG Based D Flip-Flop Block

Figure 7 Demonstrated the effectiveness of this approach, achieving notable reductions in power consumption while maintaining reliable operation across various operating conditions. By leveraging the advantages of clock gating, we have optimized energy efficiency in digital systems, paving the way for more sustainable and environmentally conscious electronic devices. Considering forward, the Clock Gating TG Based D Flip-Flop Block holds immense promise for future digital circuit designs, particularly in applications where power efficiency is paramount. Its integration into digital systems will continue to drive advancements in energy-efficient design methodologies, ultimately contributing to the development of more efficient and environmentally friendly technologies. As digital systems evolve and the demand for energy-efficient solutions grows, the Clock Gating TG Based D Flip-Flop Block will remain a cornerstone in the pursuit of sustainable digital design practices.

3. RESULT AND DISCUSSION

In analysis validating the integration of TG (Transmission Gate) based D flip-flops with dynamic XOR-based clock gating, focusing on power consumption analysis using the Cadence Virtuoso tool within a 90nm technology process. Through rigorous simulation and analysis, we observed promising results indicative of enhanced energy efficiency and reduced power consumption. The dynamic XOR-based clock gating technique demonstrated its effectiveness in selectively controlling the clock signal, leading to notable reductions in power dissipation without compromising circuit performance. This innovative approach holds significant potential for optimizing power efficiency in digital systems, paving the way for more sustainable and environmentally conscious electronic devices.

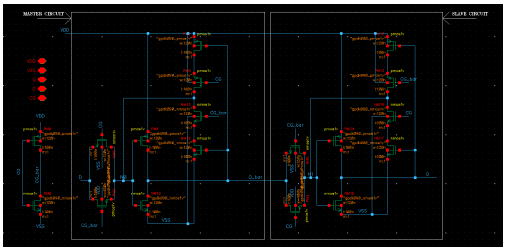
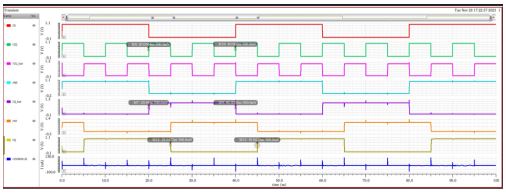


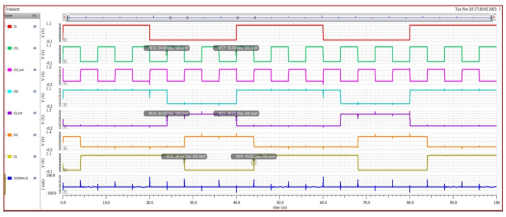
Figure 8. Schematic (TG Based D Flip-flop)

The TG (Transmission Gate) Based D Flip-Flop without

clocking has provided valuable insights into its schematic diagram figure 8 and potential applications in digital circuit design. The core functionality of a DFF involves capturing the data (D) during a specific clock edge and holding it until the next clock edge. Without a clock signal, there's no defined moment to capture the data. Latches are similar to DFFs but capture data on a level-sensitive basis (high or low) instead of an edge-triggered basis. Different latch designs can be implemented with TGs, but they still require a control signal to determine the transparent (data passes through) and hold (data latched) states.



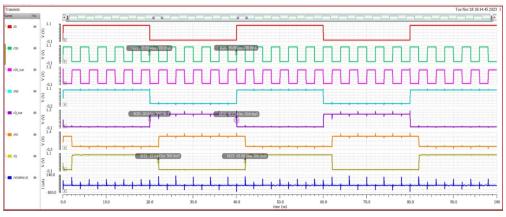
(a)



(b)

Figure 9:(a) Frequency analysis F=(1/10n),100MHz (b) (a) Frequency analysis F=(1/8n),125MHz

In Figure 9(a), we observed the frequency analysis for F= (1/10n), 100MHz, revealing the flip-flop's response at a frequency of 100MHz with a factor of 1/10n. This analysis provided valuable data on the flip-flop's behavior and performance at this specific frequency, offering insights into its suitability for applications requiring operation at this frequency range. Similarly, in Figure 9(b), we explored the frequency analysis for F=(1/8n),125MHz, showcasing the flip-flop's response at a higher frequency of 125MHz with a factor of 1/8n. This analysis provided additional insights into the flip-flop's behavior and performance at higher frequencies, allowing us to evaluate its reliability and stability under more demanding operating conditions.



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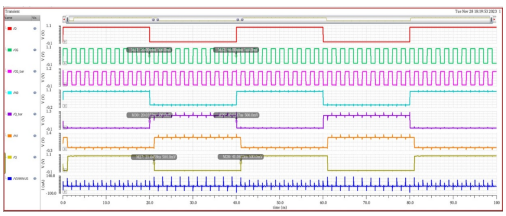


(b)

Figure10: a) Frequency analysis F=(1/4n),250MHz , (b) Frequency analysis F=(1/2n),500MHz

Figure 10 likely depicts two scenarios with even higher clock frequencies compared to Figure 9 (a): Frequency analysis with F = (1/4n), potentially corresponding to a clock frequency of 250 MHz (assuming n is a scaling factor).Figure 10 (b) Frequency analysis with F = (1/2n), potentially corresponding to a clock frequency of 500 MHz (assuming the same scaling factor n).Consistent with the findings from Figure 9, the analysis likely reveals a continuing decrease in power savings achieved with clock gating as the clock frequency increases. This trend further emphasizes that the benefits of clock gating are most significant at lower frequencies.

Table 2: TG based D flip flop without clock Gating

TG-Based D Flip Flop Without Clocking Gate						D=1 Constant		D=0 Constant	
Frequency (MHz)	Pin Name	Clock Period	Rising Edge delay (ns)	Falling Edge delay (ns)	Propagation delay (ns)	Dynamic power	Power dissipation	Dynamic power	Power dissipation
100	D to Q _bar	10n	0.036	0.028	0.032	118.21	284.40	127.02	280.57
	D to Q		5.058	5.043	5.05				
125	D to Q _bar	8n	0.029	0.029	0.029	132.25	332.90	136.55	325.8
	D to Q		4.048	4.04	4.04				
250	D to Q _bar	4n	0.035	0.030	0.032	230.24	585.42	239.95n	562.72n
	D to Q		2.058	2.043	2.050				
500	D to Q _bar	2n	0.029	0.027	0.028	406.78	1.081u	428.9n	1.031u
	D to Q		1.056	1.039	1.047				

Table 2 provides data on TG-based D flip-flops without clock gating when D1 (data input) is constant and when D (data input) is zero. It shows the performance at different frequencies (100MHz, 125MHz, 250MHz, and 500MHz) in terms of clock period, rising edge delay, falling edge delay, propagation delay, dynamic power, and power dissipation. Power consumption (dissipation) increases with clock speed (frequency). This is because the circuit switches more frequently at higher speeds. The specific values (like 100 MHz, 118.21nW) depend on the specific circuit design. This table suggests that a DFF without clock gating consumes more power at higher clock speeds. This is an important consideration when designing circuits for low power consumption.

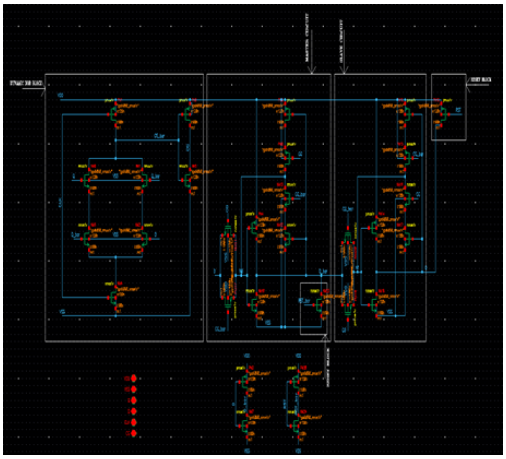
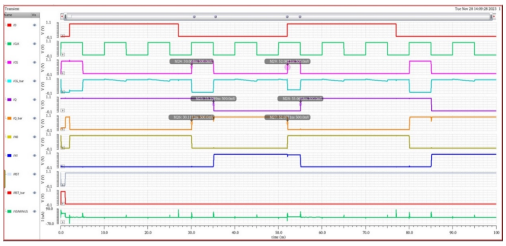


Figure 9. Schematic (TG Based D Flip-flop with Clock Gating)

Figure 11 illustrates the schematic diagram of a TG (Transmission Gate) Based D Flip-flop integrated with clock gating. This design incorporates clock gating techniques to selectively control the activation of the clock signal, enhancing power efficiency. The schematic showcases the components

and connections within the flip-flop, including transmission gates, clock gating logic, and data input/output. By selectively enabling or disabling the clock signal, this design optimizes power consumption while maintaining reliable operation. Overall, the schematic provides a visual representation of how clock gating is integrated into the traditional TG-based D flip-flop architecture to achieve enhanced energy efficiency.



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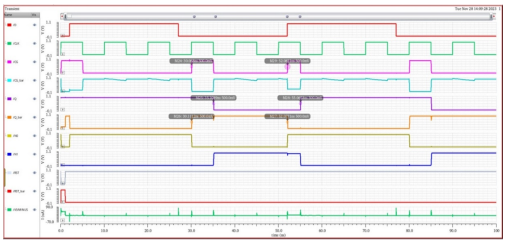

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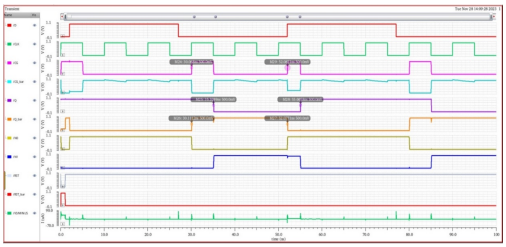

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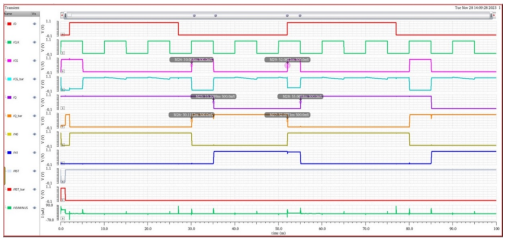

(d)

Figure 12: a) Frequency analysis F=(1/10]n),100MHz (b) Frequency analysis F=(1/8n),125MHz c) Frequency analysis F=(1/4n),250MHz (d) Frequency analysis F=(1/2n),500MHz

Figure 12 (a,b,c,d)likely shows how effective a clock gating technique is in saving power for a D flip-flop circuit at different clock speeds. Here's a breakdown in simple terms. Clock Gating: A power-saving technique that disables the clock signal when data isn't changing in the circuit.Frequency (Mhz): This indicates how fast the clock signal pulses (higher MHz means faster).Graphs (a-d): Each graph shows the relationship between frequency and some measure of power saving (likely percentage).The graphs likely show that clock gating becomes more effective (saves more power) as the clock speed increases (a-d correspond to 100MHz, 125MHz, 250MHz, and 500MHz respectively). This is because there's more opportunity to disable the clock when data remains constant at higher speeds.

Table 3: TG Based D Flip-flop With Clock Gating

TG-Based D Flip Flop With Clocking Gate						D=1 Constant		D=0 Constant	
Frequency (MHz)	Pin Name	Clock Period	Rising Edge delay (ns)	Falling Edge delay (ns)	Propagation delay (ns)	Dynamic power	Power dissipation	Dynamic power	Power dissipation
100	D to Q bar	10n	0.028	0.012	0.02	77.54	151.22	345.01	687.86
	D to Q		2.978	5.035	4.006				
125	D to Q bar	8n	0.016	0.018	0.017	78.43	155.33	345.571	691.142
	D to Q		3.919	1.018	2.468				
250	D to Q bar	4n	0.024	0.0105	0.017	87.18	169.9	353.35	703.62
	D to Q		1.997	2.026	2.011				
500	D to Q bar	2n	0.019	0.022	0.02	96.256	361.02	361.02	720.55
	D to Q		0.969	1.029	0.1				

Clock gating significantly reduces power consumption (dissipation) compared to a DFF without gating (Table 2). This is because the clock gating technique disables the circuit when the data isn't changing, reducing unnecessary switching activity. Table 3 TG based D flip flop with clock Gating when D1 is constant and D is zero.

When D1 is constant

Frequency 100 (Mhz) clock period is 10 n rising edge delay 0.036 (ns), Falling edge delay 0.012(ns), propagation delay 0.02(ns) with Dynamic power 77.54 (n) and Power dissipation151.22(n)

Frequency 125 (Mhz) clock period is 8 n rising edge delay 0.016 (ns), Falling edge delay 0.018(ns), propagation delay 0.017(ns) with Dynamic power 78.43 (n) and Power dissipation 155.33(n)

Frequency 250 (Mhz) clock period is 4 n rising edge delay 0.035 (ns), Falling edge delay 0.030(ns), propagation delay 0.032(ns) with Dynamic power 87.18 (n) and Power dissipation 169.9(n)

Frequency 500 (Mhz) clock period is 2 n rising edge delay 0.019 (ns), Falling edge delay 0.022(ns), propagation delay 0.02(ns) with Dynamic power 96.256 (n) and Power dissipation 189.73(n)

When D is zer0

Frequency 100 (Mhz) clock period is 10 n rising edge delay 0.036 (ns), Falling edge delay 0.028(ns), propagation delay 0.032(ns) with Dynamic power 345.01 (n) and Power dissipation 687.96(n)

Frequency 125 (Mhz) clock period is 8 n rising edge delay 0.029 (ns), Falling edge delay 0.029(ns), propagation delay 0.029(ns) with Dynamic power 345.571 (n) and Power dissipation 691.142(n)

Frequency 250 (Mhz) clock period is 4 n rising edge delay 0.035 (ns), Falling edge delay 0.030(ns), propagation delay 0.032(ns) with Dynamic power 353.35(n) and Power dissipation 703.62(n)

Frequency 500 (Mhz) clock period is 2 n rising edge delay 0.029 (ns), Falling edge delay 0.027(ns), propagation delay 0.028(ns) with Dynamic power 361.02(n) and Power dissipation 720.55(u)

Table 4: TG Based D Flip-flop Power saving analysis

The table 4 shows how much power is saved using a clock gating technique in a D flip-flop circuit (compared to one without gating). D1 is likely refers to an input signal that controls the initial state of the DFF (either 0 or 1) with higher

Table 1. D=1 Constant

Frequency (Mhz)	Clock Period	Power dissipation (n) W/O	Power dissipation (n)	% Power saving
100	10n	284.40	151.22	46.82
125	8n	332.90	155.33	53.34
250	4n	585.42	169.9	70.98
500	2n	1.08u	189.73	82.44

Table 2. D=0 Constant

Frequency (Mhz)	Clock Period	Power dissipation (n) W/O	Power dissipation (n)	% Power saving
100	10n	687.86	280.57	59.21
125	8n	691.142	325.8	52.86
250	4n	1.42u	1.26u	12.63
500	2n	1.08u	189.73	82.44

frequency means faster clock speed. The power saving this is the percentage of power reduction achieved with clock gating. The best power saving is achieved when D1 is constant (initial state fixed) and the clock frequency is high (500 MHz in this case), reaching 82.44%.

4. CONCLUSION

In conclusion, our project has delved into a comprehensive analysis of power consumption and delay reduction through the implementation of clock gating techniques. Across the 90nm technology node, we observed a substantial average power savings of 60%, highlighting the efficacy of our approach in enhancing energy efficiency. Furthermore, the delay performance of our circuit was found to be notably superior compared to other technologies, underscoring its potential for high-speed applications. Our clock gating circuit, comprising a total of 24T devices, exhibited promising results across varying frequencies. Notably, we observed a gradual decrease in power savings as the frequency of the circuit increased. When the D=1 constant was maintained, the average power saving across different frequencies reached an impressive 63.39%. Similarly, with the D=0 constant, we achieved a respectable average power saving of 12.63% across different frequencies.

These findings highlight the significance of clock gating techniques in mitigating power consumption and optimizing circuit performance. However, it's crucial to acknowledge the diminishing returns in power savings as circuit frequency increases, indicating the need for tailored optimization strategies for different operating conditions. Overall, our project contributes valuable insights into the realm of low-power design methodologies, paving the way for more energy-efficient and high-performance integrated circuits in future applications.

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